Preliminary Data Sheet

SV6358

Single-chip IEEE 802.11b/g/n/ax WLAN and BLE Combo SoC with USB and SDIO Interface

General Description

The SV6358 is a fully integrated SoC with 2.4GHz band 1T1R 11b/g/n/ax Wi-Fi, Bluetooth Low Energy 5.0, and MCU. A single chip MCU SoC targets for applications requiring optimal RF performance, strong security, low power consumption, and small form-factor with minimal external components. Equipped with a proven popular SDK, the SV6358 provides customers a fast time to market solution by leveraging existing software eco system, and still keep possibilities for product differentiation.

The SV6358 supports BLE Master, Slave, Advertiser, Scanner roles. It supports standard HCI in BLE side.

The SV6358 integrated the Balun, T/R switch, LNA, PA with advanced architecture enhancement to achieve great receive sensitivity for noisy home scenarios.

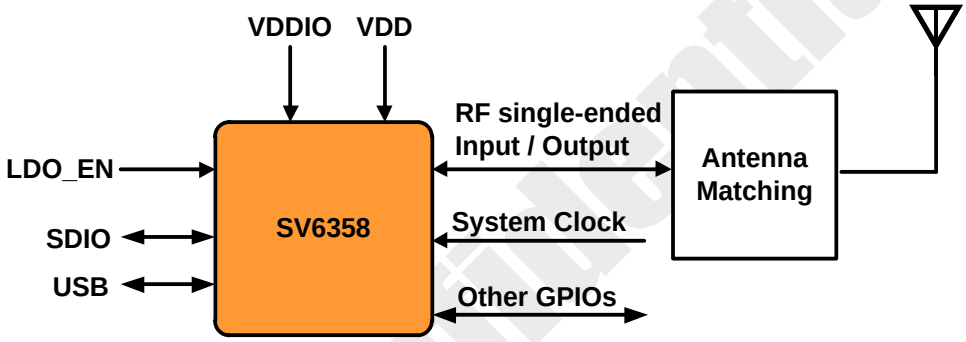
The SV6358 has additional LDOs that could provide noise isolation in between digital and analog domains minimizing external Bill of Material (BoM).

The SV6358 features an application processor subsystem based on Andes N10 32-bit RISC which runs at up to 320MHz. The chip includes up to 324KB of embedded SRAM, split among N10s local TCMs and system SRAM.

The SV6358 has a built-in hardware crypto engine, and a 1024b e-fuse block for storing chip-specific information. This combining with high efficiency security middleware library, including Wi-Fi WPA3, the SV6358 builds strong secure system products for smart home applications.

SV6358 Key Points

- IEEE 802.11 b/g/n/ax compliant
- Bluetooth 5.0
- TX power +19 dBm (at pin)
- RX sensitivity -96.5 dBm (at pin)
- Single power supply, 3.3V
- Security subsystem
  - AES HW crypto engine
  - 1024b e-fuse, TRNG
  - support Wi-Fi Alliance WPA3
- CPU core speed up to 320MHz
- Internal SRAM up to 324KB
- Support 24/26/40 MHz crystal oscillator
- Internal 32.768 KHz RC clock with calibration
- Package: QFN32, 4x4 mm, 0.4mm pitch
- Temperature range: -40°C to +85°C



SV6358 System Block Diagram

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Revision History

Version	Date	Description
0.1	2022/04/19	Initial draft
0.2	2022/06/07	Add RF performance and power consumption data

Table of Contents

Lists of Tables

Lists of Figures

1 System Overview

1.1 System Block Diagram

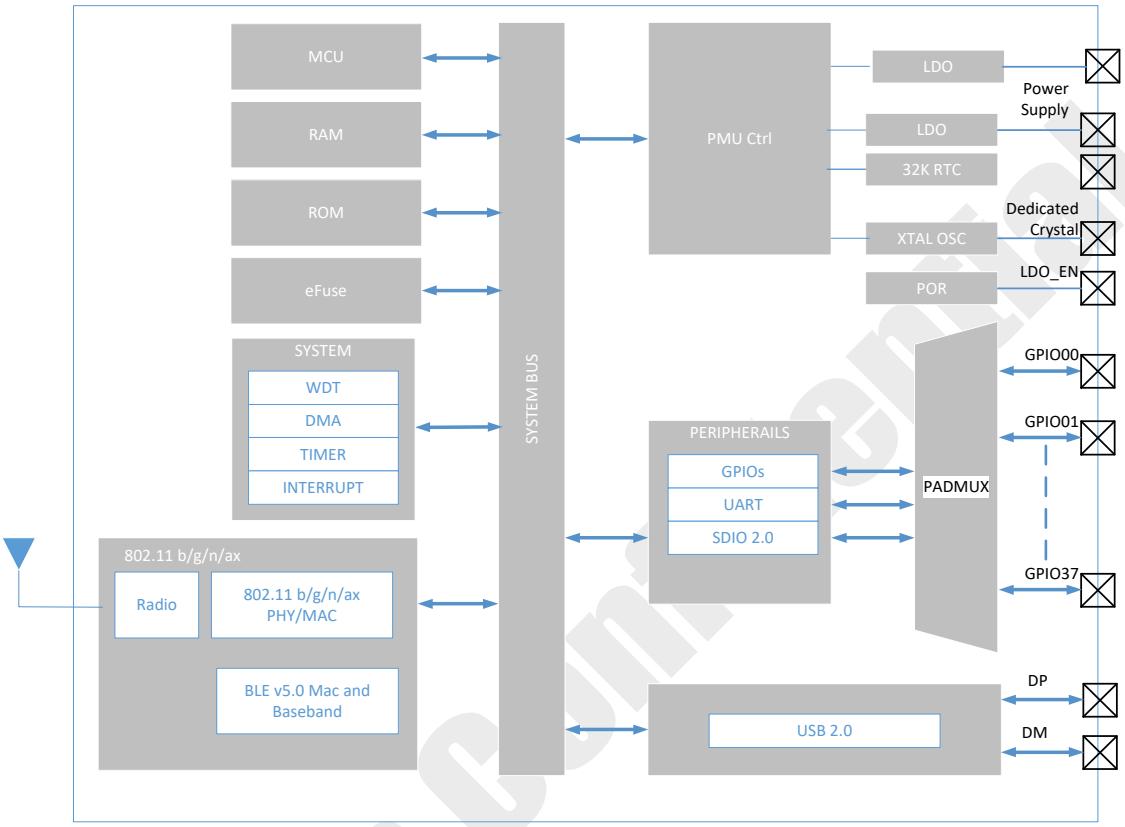

Figure 1: SV6358 Block Diagram

1.2 General Description

The SV6358 WLAN SoC is designed to support IEEE 802.11 b/g/n/ax single spatial stream and Bluetooth 5.0 It is designed with the state of-the-art techniques and process technology to achieve low power consumption and high throughput performance to address the requirement of mobile and handheld devices. The SV6358 WLAN low power function uses the innovative design techniques and the optimized architecture which best utilizes the advanced process technology to reduce active and idle power, and to achieve extreme low power consumption at sleep state to extend the battery life. The SV6358 WLAN A-MPDU Tx function maximizes the throughput performance while achieving the best buffer utilization.

The Bluetooth subsystem contains the Bluetooth radio, modem, and link controller.

1.3 WLAN FEATURES

- IEEE 802.11 b/g/n/ax 1T1R compliant
- IEEE 802.11 d/e/i/w supported
- Support 802.11n 20/40MHz up to MCS7 150Mbps
- Support 802.11ax 20/40MHz up to MCS9 229Mbps
- 802.11n features supported
  - A-MPDU Tx & Rx for high MAC throughput
  - Support immediate Block-Ack
- STA, SoftAP and Sniffer modes supported
- Concurrent AP + STA supported
- Ad-hoc, peer-to-peer and Wi-Fi Direct modes supported
- Low power Tx/Rx for short range scenario
- Low power beacon listen mode
- Low power dormant mode
- WFA features
  - WEP/WPA/WPA2/WPA3
  - WMM
- Short Guard Interval for 802.11ax optimal performance
- Greenfield mode for 802.11ax optimal performance
- STBC in RX mode
- LDPC
- Tx power: +19 dBm
- Rx sensitivity: -96.5 dBm
- Integrated Balun, T/R switch, LNA and PA for 2.4GHz
- Enhanced and robust sensitivity for wider coverage range
- Supports calibration algorithm to handle non-ideal effects from CMOS RF block

1.4 BLUETOOTH FEATURES

- Bluetooth 5.0 Low Energy
- Integrated Balun and PA
- High power mode: up to 10 dBm
- Rx sensitivity: -98 dBm
- Channel assessment for AFH
- Internal co-existence scheme between Wi-Fi and Bluetooth
- Concurrent slave/advertiser/scanner operations supported
- Master mode supported
- SIG Mesh v1.01 supported
- GATT and Mesh profile
- Device Provision Protocol (DPP) with BLE 5.0 Extended Advertising supported

1.5 SYSTEM

- Andes Technology N10 processor w/ ILM/DLM and I-cache
- Dedicated 8KB I-cache supported
- Memory Protection Unit (MPU) supported
- 188KB ROM and up to 320KB SRAM for Instruction and data SRAM in total

- Low power Dormant mode
- Low power Shut-Down mode
- Security and encryption
- AES hardware acceleration
- Integrated True Random Number Generator
- Integrated 1024b e-fuse
- Suspend/Wake-up manger controller
- 1 DMA, each with 5 channels
- Four millisecond timers
- Four microsecond timers
- Two watchdog timers

1.6 HOST INTERFACE

- SDIO 2.0
  - 1bit/4bits mode supported
  - Support Clock up to 50MHz
- USB 2.0
  - High speed / Full speed / Low speed supported
  - Suspend / Selected suspend supported

1.7 SYSTEM CLOCKING AND RESET

The SV6358 has a system clocking block and reset which controls the clocks and power going to other internal modules. Its inputs consist of sleep requests from these modules and its outputs consist of clock enable and power signals which are used to gate the clocks going to internal modules. The system clocking and reset block also manages resets going to other modules within the device.

1.8 DESIGN FOR TEST

It also has features which enable testing of digital blocks via ATPG scan, memories via MBIST, analog components, and the radio.

2 Power Supplies and Power Management

2.1 General Description and PMU Power Connection

The power management unit (PMU) contains Low Dropout Regulators (LDOs), and reference bandgap circuit.

The PMU integrates multi-LDOs. Those circuits are optimized for the given functions by balancing quiescent current, dropout voltage, ripple rejection and output noise.

The input voltage of the LDO is 3.3V. Its output voltage is 1.1V and feeds into the input power of the RF circuit and DLDO which has 0.8V output voltage for all digital circuits.
Figure 2 shows the typical power connection for SV6358. DLDO and some RF circuits are powered by the LDO output. The VDDIO is a power input which may be 1.8V or 3.3V from the host side. The connection structure is shown in the Figure 2

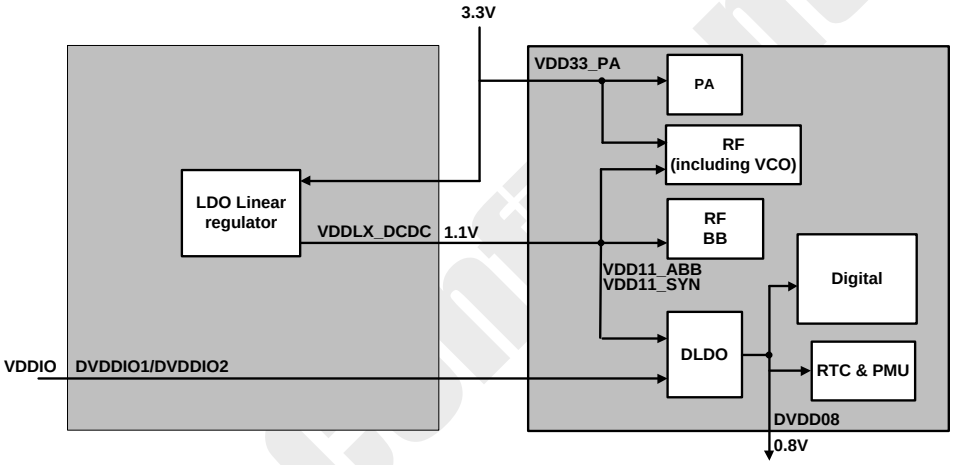

Figure 2: SV6358 Power Connection

2.2 DLDO

The DLDO is integrated in the PMU to supply digital core. It converts voltage from 1.1V input to 0.8V output which suits the digital circuits. The input is typically connected to the buck's output.

2.3 LDO Linear Regulator

The regulator is linear regulator to source 300 mA (max.) with 1.3V to 1.05V programmable output voltage based on the register setting. It supplies power for the RF circuit and DLDO.

2.4 Power-on Sequence

2.4.1 Power-on Sequence with typical power

Figure 3 shows the power-on sequence of the SV6358 from power-up to firmware download, including the initial device power-on reset evoked by internal LDO_EN signal. After initial power-on, the LDO_EN signal can be held low to turn off the SV6358 or pulsed low to induce a subsequent reset.

After LDO_EN is asserted, the host starts the power-on sequence of the SV6358. From that point, the typical SV6358 power-on sequence is shown below:

1. Within T1+2.5ms, the internal power-on reset (POR) will be done. And host could download firmware code of DPLL setting if the crystal is not default setting, 26MHz. The internal running clock is crystal frequency.
2. After 100us of DPLL settling time, host could set internal clock to full speed and finish all the downloading of firmware code.

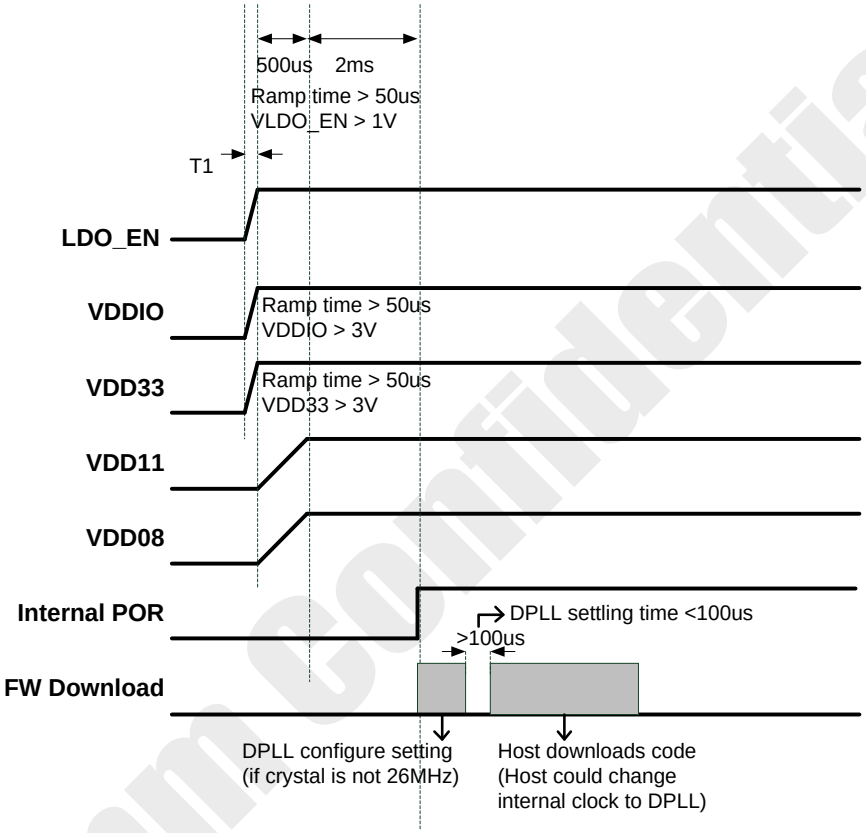

Figure 3: Power-on sequence with typical power

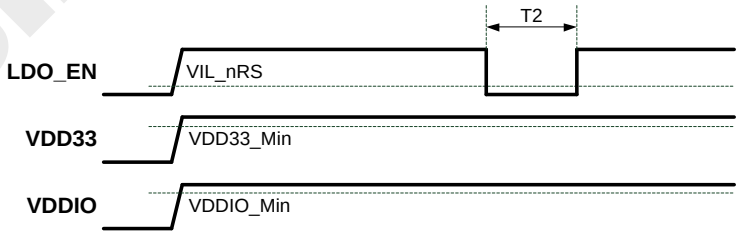

Figure 4: Reset Timing with typical power

Table 1: Reset Timing Parameters

Parameters	Description	Min.	Unit
T_2	Duration of LDO_EN signal level < VIL_Nrst(refer to its value in Table 11: Recommended Operating Conditions and DC Characteristics) to reset the chip	500	us

2.5 RESET CONTROL

The SV6358 **LDO_EN** pin can be used to completely reset the entire chip. After this signal has been de-asserted, the SV6358 is in off mode waiting for host communication. Until then, the MAC, Baseband modem, and MCU subsystem blocks are powered off and all modules are held in reset. Once the host has initiated communication, the SV6358 turns on its crystal and later on DPLL. After all clocks are stable and running, the resets to all blocks are automatically de-asserted.

3 Interface Description

3.1 SDIO Characteristics

SDIO is compliant to SDIO specification version 2.0, supporting 1-bit and 4-bit data transfer mode, and compliant to high speed SD Bus

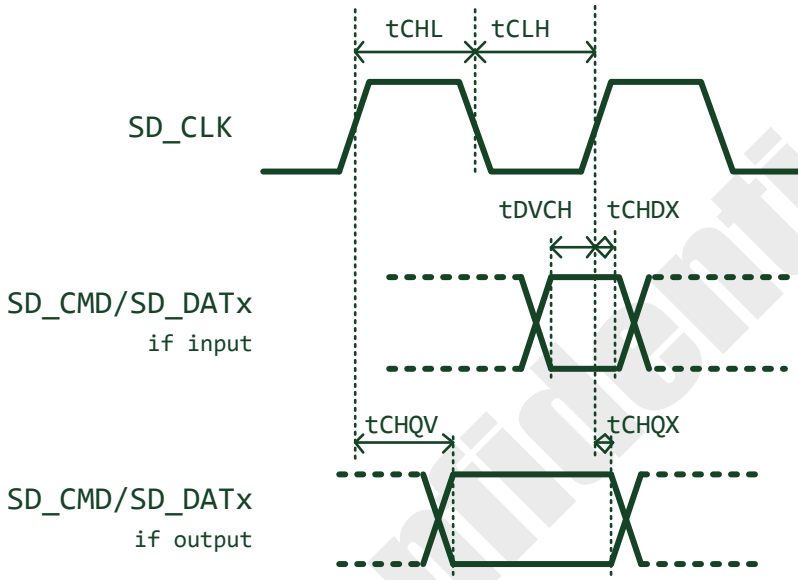

Figure 5: SDIO Timing

Table 2: SDIO Timing Specifications

Parameter	Condition/Notes	Min.	Typ.	Max.	Unit
SDIO clock frequency	–	(TBD)		50	MHz
SDIO clock high time	Tchl	7	–	-	ns
SDIO clock low time	Tclh	7	-	-	ns
SDIO input setup time	Tdvch	6	-	-	ns
SDIO input hold time	Tchdx	2	-	-	ns
SDIO output delay	Min.: Tchqx, Max.: Tchqv	2.5	-	14	ns

3.2 USB Characteristics

Table 3 : USB High-Speed Source Electrical Characteristics

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
Driver characteristics						
tHSRLEW	Slew rate of rising edge	-	-	-	1600	V/usec
tHSFLEW	Slew rate of falling edge	-	-	-	1600	V/usec
Driver waveform	-	Specified by eye pattern template in	-	-	-	-

		USB2.0 spec.				
Clock Timings						
THSRDRATE	High-speed data rate		479.76	-	480.24	Mbps
High-Speed Data Timings						
TJ	Data source jitter	Source and receiver jitter specified by the eye pattern template defined in USB2.0 spec.				
RXJT	Receiver jitter tolerance					

Table 4: USB Full-Speed Source Electrical Characteristics

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
Driver characteristics						
tFR	Rise time	CL = 50 pF 10% ~ 90% of |VOH – VOL|	4	-	20	ns
tHSFLEW	Fall time	CL = 50 pF 90% ~ 10% of |VOH – VOL|	4	-	20	ns
tFRMA	Differential rise/fall time matching (tFR/tFF)	Specified by eye pattern template in USB2.0 spec.	90	-	110	%
Clock Timings						
TFSTXDRATE	Full-speed TX data rate		11.994	-	12.006	Mbps
TFSRXDRATE	Full-speed RX data rate		11.97	-	12.03	Mbps
Full-Speed Data Timings						
TFDEOP	Source jitter for differential transition to SE0 transition	-	-2	-	5	ns
TJR1	Receiver jitter	To next transition	-18.5	-	18.5	ns
TJR2	Receiver jitter	For paired transition	-9	-	9	ns
TFEOPT	Source SE0 interval of EOP	-	160	-	175	ns
TFEOPR	Receiver SE0 interval of EOP	-	82	-	-	ns
TFST	Width of SE0 interval during differential transition	-	-	-	14	ns

Table 5 : USB Low-Speed Source Electrical Characteristics

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
Driver characteristics						
tFR	Rise time	CL = 200 pF~ 600 pF 10% ~ 90% of |VOH–VOL|	75	-	300	ns
tHSFLEW	Fall time	CL = 200pF ~ 600pF 90% ~ 10% of |VOH–VOL|	75	-	300	ns
tFRMA	Differential rise/fall time matching (tFR/tFF)	Specified by eye pattern template in USB2.0 spec.	80	-	125	%
Clock Timings						
TFSTXDRATE	Low-speed TX data rate		1.49925	-	1.50075	Mbps
TFSRXDRATE	Low-speed RX data rate		1.49925	-	1.50075	Mbps
Low-Speed Data Timings						
TFDEOP	Source jitter for differential transition to SE0 transition	-	-40	-	100	ns
TJR1	Receiver jitter	To next transition	-75	-	75	ns
TJR2	Receiver jitter	For paired transition	-45	-	45	ns
TFEOPT	Source SE0 interval of EOP	-	1.25	-	1.5	ns
TFEOPR	Receiver SE0 interval of EOP	-	670	-	-	ns
TFST	Width of SE0 interval during differential transition	-	-	-	210	ns

4 DC CHARACTERISTICS

4.1 ABSOLUTE MAXIMUM RATINGS

The absolute maximum ratings in Table 6 indicate levels where permanent damage to the device can occur, even if these limits are exceeded for only a brief duration. Functional operation is not guaranteed under these conditions. Operation at absolute maximum conditions for extended periods can adversely affect long-term reliability of the device.

Table 6: Absolute Maximum Ratings

Symbol (domain)	Description	Max Rating	Unit
AVDD11_SX	VDD input for analog 1.1V	-0.3 to 1.8	V
AVDD11_RF	VDD input for analog 1.1V	-0.3 to 1.8	V
AVDD33_SX	VDD input for external components I/O control	-0.3 to 3.6	V
AVDD33_PA	VDD input for external components I/O control	-0.3 to 3.6	V
AVDD33_TX	VDD input for external components I/O control	-0.3 to 3.6	V
DVDDIO1	VDD input for GPIO pins	-0.3 to 3.6	V
DVDDIO2	VDD input for GPIO pins	-0.3 to 3.6	V
DVDD08_DIG	VDD output for internal digital circuit	-0.3 to 1.0	V
DVDD11_DIG	VDD input for digital circuit's LDO	-0.3 to 1.4	V
AVDD33_DCDC	VDD input for DCDC	-0.3 to 3.6	V

4.2 ENVIRONMENTAL RATINGS

The environmental ratings are shown in Table 7

Table 7: Environmental Ratings

	Part Number	Value	Units
Operating Temperature(T_A)	SV6358	-40 to +85	°C

4.3 STORAGE CONDITION

The calculated shelf life in sealed bag is 12 months if stored between 0°C and 40°C at less than 90% relative humidity (RH). After the bag is opened, devices that are subjected to solder reflow or other high temperature processes must be handled in the following manner:

a) Mounted within 168-hours of factory conditions < 30 **°C** /60%RH
b) Storage humidity needs to maintained at <10% RH
c) Baking is necessary if customer exposes the component to air over 168 hours, baking condition: 125°C / 8hours

4.4 THERMAL CHARACTERISTICS

Table 8: The thermal characteristics of the SV6358

Thermal characteristics without external heat sink in still air condition

Symbol	Description	Typ.	Unit
T_J	Maximum Junction Temperature (Plastic Package)	125	°C
θ_{JA}	Thermal Resistance θ_{JA} (°C /W) for JEDEC 4L system PCB	59.9	°C/W
θ_{JC}	Thermal Resistance θ_{JC} (°C /W) for JEDEC 4L system PCB	40.1	°C/W
Ψ_{Jt}	Thermal Characterization parameter Ψ_{Jt} (°C /W) for JEDEC 4L system PCB	0.8	°C/W
	Maximum Lead Temperature (Soldering 10s)	260	°C

Notes: * JEDEC 51-7 system FR4 PCB size: 3” x 4.5” (76.2 x 114.3 mm)

* Thermal characteristics without external heat sink in still air condition

4.5 ESD RATING

Table 9: ESD Rating

ESD Mode	Standard	Value	Unit
Human Body Mode (HBM)	JEDEC EIA/JESD22-A114	TBD	V

JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process

4.6 POWER-ON HOURS(POH)

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Table 10: Power-On Hours

OPERATION CONDITION	Part Number	Power-On Hours(POH)(hours)
T_A up to 85°C [a]	SV6358	87600

a. The TX duty cycle (power amplifier ON time) is assumed to be 10% of the device POH. Of the remaining 90% of the time, the device can be in any other state.

4.7 Recommended Operating Conditions and DC Characteristics

Table 11: Recommended Operating Conditions and DC Characteristics

Domain (Symbol)	Description	Min.	Typ.	Max.	Unit
AVDD11_SX	VDD input for analog 1.1V	0.9	1.1	1.3	V
AVDD11_RF	VDD input for analog 1.1V	0.9	1.1	1.3	V
AVDD33_SX	VDD input for external components I/O control	2.1	3.3	3.46	V
AVDD33_PA	VDD input for external components I/O control	2.1	3.3	3.46	V
AVDD33_TX	VDD input for external components I/O control	2.1	3.3	3.46	V
DVDDIO1	VDD input for GPIO pins	1.75	3.3	3.46	V
DVDDIO2	VDD input for GPIO pins	1.75	3.3	3.46	V
DVDD08_DIG	VDD output for internal digital circuit		0.8		V
DVDD11_DIG	VDD input for digital circuit's LDO		1.1		V
AVDD33_DCDC	VDD input for DCDC	2.1	3.3	3.46	V
(V_{IL})	Input Low voltage when VDDIO=3.3V	-0.3		0.8	V
(V_{IH})	Input High voltage when VDDIO=3.3V	2		3.6	V
(V_{T+})	Schmitt trigger low to high threshold voltage when VDDIO=3.3V	1.52	1.63	1.77	V
(V_{T-})	Schmitt trigger high to low threshold voltage when VDDIO=3.3V	1.29	1.41	1.56	V
(V_{OL})	Output low voltage when VDDIO=3.3V			0.4	V
(V_{OH})	Output high voltage when VDDIO=3.3V	2.4			V
(R_{PD})	Input weakly pull-down resistance when VDDIO=3.3V. All GPIO pins have internal weakly pull-down option except that GPIO_5 has internal weakly pull-up option				KΩ
(R_{PU})	Input weakly pull-high resistance when VDDIO=3.3V. All GPIO pins have internal weakly pull-down option except that GPIO_5 has internal weakly pull-up option				KΩ
VIH_Nrst	Chip reset release voltage		>1		V
VIL_Nrst	Chip reset voltage		<0.1		V

(I_{OL})	Low level output current @ V_{OL}(max), 8 mA setting	5.2	7.52	10.09	mA
	Low level output current @ V_{OL}(max), 12 mA setting	10.4	15.03	20.2	mA
(I_{OH})	High level output current @ V_{OH}(min), 8 mA setting	6.8	12.08	18.44	mA
	High level output current @ V_{OH}(min), 12 mA setting	12.7	22.64	35.09	mA

5 FREQUENCY REFERENCES

5.1 CRYSTAL OSCILLATOR SPECIFICATIONS

Table 12: Crystal Oscillator Specifications

Parameter	Condition/Notes	Min.	Typ.	Max.	Unit
Frequency	–	24/26/40 MHz			
Crystal load Capacitance	–	–	10		Pf
ESR	–	–	–	70	Ω
Frequency tolerance Initial and over temperature	–	-20	–	20	ppm

5.2 EXTERNAL CLOCK-REQUIREMENTS AND PERFORMANCE

Table 13: External Clock-Requirements and Performance

Parameter	Condition/Notes	Min.	Typ.	Max.	Unit
Frequency	–	24/26/40 MHz			
OSCIN Input Voltage	AC-couple analog signal	400	–	900	mV_{PP}
Frequency tolerance Initial and over temperature	–	-20	–	20	ppm
Duty Cycle	26MHz clock	40	50	60	%
Phase Noise (802.11b/g)	26MHz clock at 1KHz offset	–	–	–119	dBc/Hz
	26MHz clock at 10KHz offset	–	–	–129	dBc/Hz
	26MHz clock at 100KHz offset	–	–	–134	dBc/Hz
	26MHz clock at 1MHz offset	–	–	–139	dBc/Hz
Phase Noise (802.11n 2.4GHz)	26MHz clock at 1KHz offset	–	–	–125	dBc/Hz
	26MHz clock at 10KHz offset	–	–	–135	dBc/Hz
	26MHz clock at 100KHz offset	–	–	–140	dBc/Hz
	26MHz clock at 1MHz offset	–	–	–145	dBc/Hz

6 ELECTRICAL SPECIFICATIONS

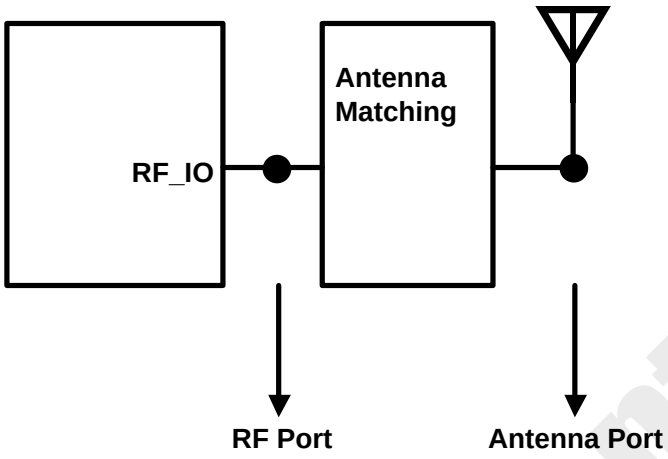


Figure 6: RF Front-End Reference Topology for RF Performance

Note: All specifications are measured at the RF Port unless otherwise specified.

6.1 WLAN RF Performance Specifications

Table 14: 2.4G WLAN RF Performance Specifications

Parameter	Condition/Notes	Min.	Typ.	Max.	Unit
Frequency Range		2412	-	2484	MHz
Rx Sensitivity (CCK)	CCK, 1 Mbps		-96.2		dBm
	CCK, 2 Mbps		-92.5		dBm
	CCK, 5.5 Mbps		-91.3		dBm
	CCK, 11 Mbps		-87.7		dBm
Rx Sensitivity (OFDM)	OFDM, 6 Mbps		-91.5		dBm
	OFDM, 9 Mbps		-90.1		dBm
	OFDM, 12 Mbps		-88.9		dBm
	OFDM, 18 Mbps		-86.7		dBm
	OFDM, 24 Mbps		-83.9		dBm
	OFDM, 36 Mbps		-80.1		dBm
	OFDM, 48 Mbps		-76.5		dBm
	OFDM, 54 Mbps		-75.2		dBm
Rx Sensitivity (HT20) Mixed mode 800Ns GI Non-STBC	MCS0		-90.7		dBm
	MCS1		-88.2		dBm
	MCS2		-85.9		dBm
	MCS3		-83.1		dBm
	MCS4		-79.7		dBm
	MCS5		-75.5		dBm
	MCS6		-74.1		dBm
	MCS7		-72.7		dBm
Rx Sensitivity (HT40) Mixed mode 800nS GI Non-STBC	MCS0		-88.3		dBm
	MCS1		-85.3		dBm
	MCS2		-82.7		dBm
	MCS3		-79.7		dBm
	MCS4		-76.5		dBm
	MCS5		-72.1		dBm
	MCS6		-70.1		dBm
	MCS7		-68.7		dBm
Rx Sensitivity (HE20) Mixed mode 800nS GI	MCS0		-90.9		dBm
	MCS1		-87.7		dBm
	MCS2		-85.9		dBm
	MCS3		-82.9		dBm
	MCS4		-79.5		dBm
	MCS5		-75.9		dBm
	MCS6		-73.9		dBm
	MCS7		-72.5		dBm
	MCS8		-67.7		dBm
	MCS9		-65.9		dBm
Rx Sensitivity	MCS0		-88.7		dBm
	MCS1		-86.9		dBm

(HE40)	MCS2		-84.1		dBm
Mixed mode	MCS3		-81.5		dBm
800nS GI	MCS4		-78.3		dBm
LDPC	MCS5		-74.5		dBm
	MCS6		-73.3		dBm
	MCS7		-71.3		dBm
	MCS8		-67.5		dBm
	MCS9		-64.9		dBm
Parameter	**Condition/Notes**	**Min.**	**Typ.**	**Max.**	**Unit**
RX Adjacent Channel Rejection (CCK)	1 Mbps		40		dB
	11 Mbps		40		dB
RX Adjacent Channel Rejection (OFDM)	6 Mbps		42.5		dB
	54 Mbps		25		dB
RX Adjacent Channel Rejection (HT20)	MCS0		38.5		dB
	MCS7		19.5		dB
RX Adjacent Channel Rejection (HT40)	MCS0		26		dB
	MCS7		9		dB
RX Adjacent Channel Rejection (HE20)	MCS0		27		dB
	MCS9		2		dB
RX Adjacent Channel Rejection (HT40)	MCS0		26		dB
	MCS9		5		dB

Parameter	Condition/Notes	Min.	Typ.	Max.	Unit
TX Output Power	CCK, 1-11 Mbps		18		dBm
	OFDM, 54 Mbps		15		dBm
	HT20, MCS7		15		dBm
	HT40,MCS7		15		dBm
	HE20,MCS9		12.5		dBm
	HE40,MCS9		12.5		dBm

6.2 BLUETOOTH RF PERFORMANCE SPECIFICATIONS

Table 15: Bluetooth RF Performance Specifications

TX Characteristic	Min.	Typ.	Max.	Unit
Frequency Range	2402	-	2480	MHz
Output power	0	6	10	dBm
Carrier Frequency Offset and Drift				
Frequency Offset	-150		150	KHz
Frequency Drift	-50		50	KHz
Max Drift Rate	-20		20	KHz/50us
Modulation Characteristic				
△f1avg	225		275	KHz
△f2max	185			KHz
△f1avg/△f2avg	0.8	0.94		
In-band Spurious Emission				
±2M Offset			-20	dBm
> ±3MHz offset			-30	dBm

RX Characteristic	Min.	Typ.	Max.	Unit
Frequency Range	2402	-	2480	MHz
Receiver Sensitivity		-98		dBm
C/I Co-channel		6.5	21	dB
C/I 1MHz		4	15	dB
C/I 2MHz		-21	-17	dB
C/I ≥3MHz		-30	-27	dB
C/I Image channel		NA		dB
C/I Image 1MHz		NA		dB
Inter-modulation	-50	-35		dBm
Out-of-band blocking				
30MHz to 2000MHz	-30			dBm
2001MHz to 2339MHz	-35			dBm
2501MHz to 3000MHz	-35			dBm
3001MHz to 12.75GHz	-30			dBm

7 System Power Consumption

Table 16: Power Consumption

WLAN Operational Modes	Typ[c]	Unit
OFF[a]	1.5	uA
Rx, CCK, 1 Mbps	107	mA
Rx, OFDM, 54 Mbps	107	mA
Rx, HT20, MCS7	107	mA
Rx, HT40, MCS7	107	mA
Tx, CCK, 1 Mbps@19dBm	318	mA
Tx, OFDM, 54 Mbps@15dBm	263	mA
Tx, HT20, MCS0@18dBm	310	mA
Tx, HT20, MCS7@15dBm	268	mA

a. OFF mode test condition: VDD=3.3V, LDO_EN=0V

b. Intra-beacon Sleep when MCU is turn off

c. Conditions: VDD=3.3V

PIN DESCRIPTIONS

7.1 PIN LAYOUT

This section contains a listing of the signal descriptions (see Figure 7 for the SV6358 package pin-out)

Figure 7: SV6358 Pin Assignment –QFN32 (top view)

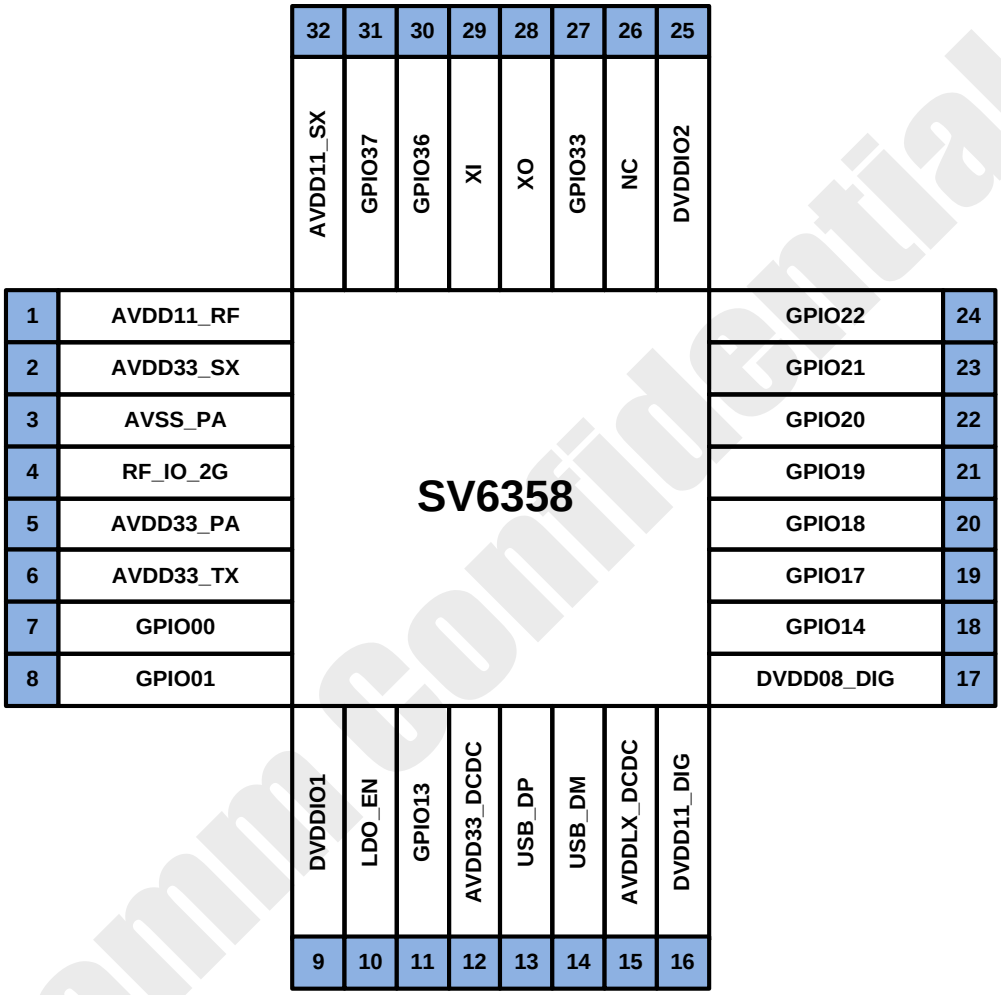


Table 17: SV6358 Pin coordination

Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name
1	AVDD11_RF	2	AVDD33_SX	3	AVSS_PA	4	RF_IO_2G
5	AVDD33_PA	6	AVDD33_TX	7	GPIO00	8	GPIO01
9	DVDDIO1	10	LDO_EN	11	GPIO13	12	AVDD33_DCDC
13	USB_DP	14	USB_DM	15	AVDDLX_DCDC	16	DVDD11_DIG
17	DVDD08_DIG	18	GPIO14	19	GPIO17	20	GPIO18
21	GPIO19	22	GPIO20	23	GPIO21	24	GPIO22
25	DVDDIO2	26	NC	27	GPIO33	28	XO
29	XI	30	GPIO36	31	GPIO37	32	AVDD11_SX

7.2 PIN DESCRIPTION

Table 18: SV6358 Package Pin-out

Pin Name	Pin No.	Type*	Description
General purpose I/O			
GPIO00	7	I/O	General Purpose I/O Pins
GPIO01	8	I/O	Strapping Purpose I/O Pins
GPIO13	11	I/O	Strapping Purpose I/O Pins
GPIO14	18	I/O	General Purpose I/O Pins
GPIO17	19	I/O	General Purpose I/O Pins
GPIO18	20	I/O	General Purpose I/O Pins
GPIO19	21	I/O	General Purpose I/O Pins
GPIO20	22	I/O	General Purpose I/O Pins
GPIO21	23	I/O	General Purpose I/O Pins
GPIO22	24	I/O	General Purpose I/O Pins
GPIO33	27	I/O	General Purpose I/O Pins
GPIO36	30	I/O	General Purpose I/O Pins
GPIO37	31	I/O	General Purpose I/O Pins
IO Power			
DVDDIO1	9	P	VIO input
DVDDIO2	25	P	VIO input
Reset and Clocks			
LDO_EN	10	I	Reset signal to power down IC
XO	28	O	Output of crystal clock reference
XI	29	I	Input of crystal clock reference
PMU/LDO/USB			
AVDD33_DCDC	12	P	analog 3.3V input for LDO
USB_DP	13	I/O	USB DP
USB_DM	14	I/O	USB_DM
AVDDLX_DCDC	15	P	LDO regulator: output
DVDD11_DIG	16	P	LDO regulator: input
DVDD08_DIG	17	P	Digital 0.8V output
Wi-Fi radio			
AVDD11_SX	32	P	analog 1.1V input
AVDD11_RF	1	P	analog 1.1V input
AVDD33_SX	2	P	analog 3.3V input
AVSS_PA	3	G	Ground
RF_IO_2G	4	I/O	2.4 GHz RF input & output port
AVDD33_PA	5	P	analog 3.3V input
AVDD33_TX	6	P	analog 3.3V input

* I=Input; O=Output; G=Ground; P=Power

7.3 Mode Selection

Table 19: Mode Selection table

strapping truth table		
GPIO13,GPIO01	**Interface mode**	**Description**
01	SDIO	SDIO mode (default)*
00	USB	Xtal = 26MHz
10	USB	Xtal = 40MHz
11	Reserve	Reserve

*No external pull-down resistor is required because internal pull-up/pull-down is active during power up.

7.4 Function Selection For SV6358 SDIO Mode

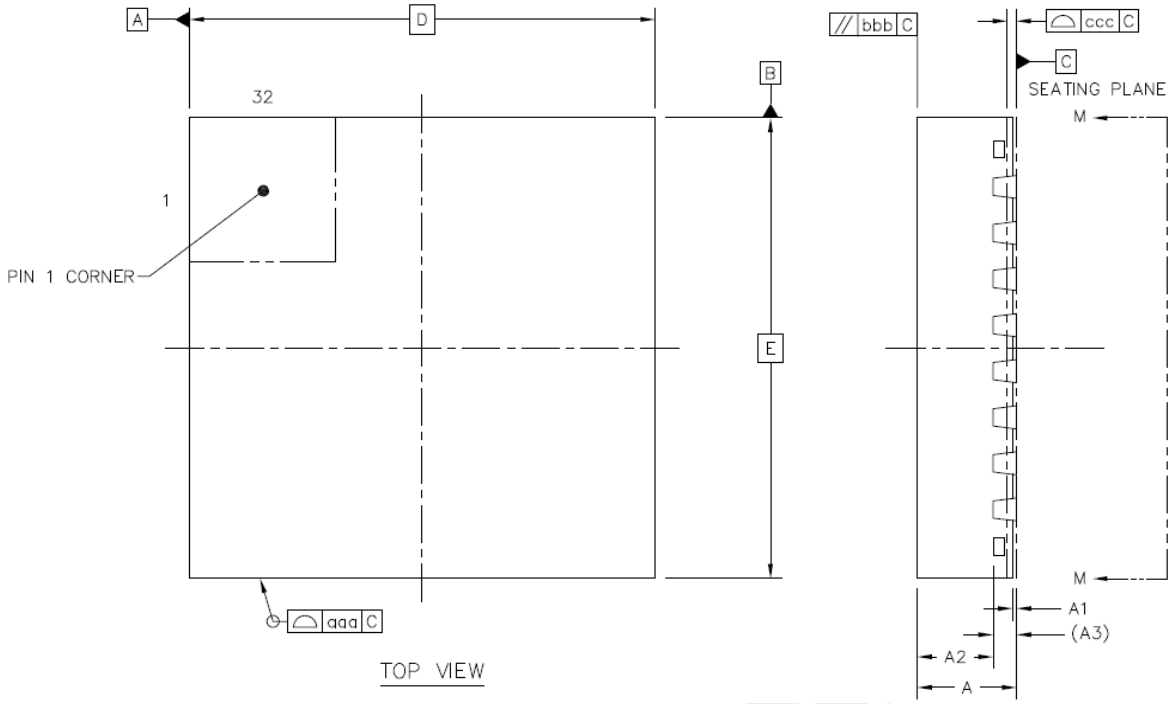
After bootstrap, the SV6358 provides a pad multiplex switching from the bootstrap function to selected I/O function by register signals. There is a condition to leave bootstrap function. That is switching to GPIO first then switching to select I/O function. The table shows the all I/O functions for each PAD.

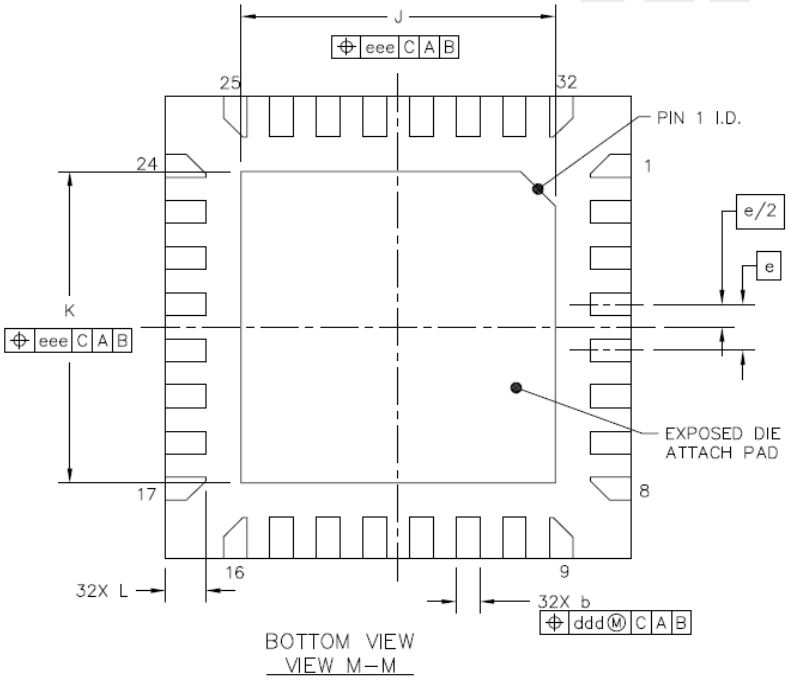
Table 20: Pinmux for SV6358 SDIO Mode

Name	Pin No.	Dir	PU/PD	SDIO
GPIO00	7	I	F	UART0_RXD
GPIO01	8	O	F	UART0_TXD, Strap
GPIO13	11	I/O	F	Strap
GPIO14	18	O	F	Wi-Fi_WAKEUP_Host
GPIO17	19	I/O	F	SD_DATA2
GPIO18	20	I/O	F	SD_DATA3
GPIO19	21	I/O	F	SD_CMD
GPIO20	22	I	F	SD_CLK
GPIO21	23	I/O	F	SD_DATA0
GPIO22	24	I/O	F	SD_DATA1
GPIO33	27	O	F	RX_IRQ(out_band)
GPIO36	30	N/A	F	UART2_RXD
GPIO37	31	N/A	F	UART2_TXD

8 PACKAGE INFORMATION

4 x 4 mm (body size), 0.4mm pitch QFN-32





		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.8	0.85	0.9
STAND OFF		A1	0	0.035	0.05
MOLD THICKNESS		A2	---	0.65	---
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.15	0.2	0.25
BODY SIZE	X	D		4 BSC	
	Y	E		4 BSC	
LEAD PITCH		e		0.4 BSC	
EP SIZE	X	J	2.6	2.7	2.8
	Y	K	2.6	2.7	2.8
LEAD LENGTH		L	0.3	0.35	0.4
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		bbb		0.1	
COPLANARITY		ccc		0.08	
LEAD OFFSET		ddd		0.1	
EXPOSED PAD OFFSET		eee		0.1	

Figure 8: QFN 4 x 4 mm Package Dimensions

9 ORDERING INFORMATION

The table below provides the ordering information of the SV6358.

Table 21: SV6358 Ordering Part Number

Part number	Package	Feature
SV6358	QFN32	Wi-Fi